What is claimed is:

1. A radiation detector comprising:

an array of memory cells;

a processor connected to said memory cells and configured to detect a bit flip in one or more of said memory cells.

2. A radiation detector in accordance with claim 1 wherein said array of memory cells comprises an array of static, random access memory cells (SRAM).

3. A radiation detector in accordance with claim 1 wherein said array of memory cells comprises a two-dimensional array.

4. A radiation detector in accordance with claim 3 further including a plurality of arrays of memory cells.

5. A radiation detector in accordance with claim 3 further including a stacked plurality of memory cells.

6. A radiation detector in accordance with claim 5 wherein said stacked plurality of memory cells comprises two stacked arrays of memory cells.

7. A radiation detector in accordance with claim 5 wherein said stacked plurality of memory cells comprises ten stacked arrays of memory cells.

8. A radiation detector in accordance with claim 1 wherein said processor is configured to detect a bit flip by

writing a predetermined pattern of 1's and 0's in said memory array; and

determining a wrong bit in said predetermined pattern.

9. A radiation detector in accordance with claim 1 wherein said array of memory cells comprises a stacked plurality of memory cells and wherein said processor is configured to further detect a direction of an ion by determining a plurality of wrong bits in said stacked plurality of memory cells.

10. A radiation detector in accordance with claim 1 wherein said radiation detector is approximately less than one cubic inch.

11. A radiation detector in accordance with claim 1 wherein said memory cells are softened to improve susceptibility to ions causing bit flips.

12. A radiation detector in accordance with claim 1 wherein said memory cells are coated with a material that reacts with radiation to generate ionization.

13. A method of detecting radiation for use in a structure comprising a processor and a plurality of layers of memory cell arrays, said method comprising:

distributing a predetermined pattern of 1's and 0's in said memory cell arrays; and

detecting a particle strike by scanning said memory cell array for a bit flip.

14. A method in accordance with claim 13 further comprising:

periodically scanning said memory cell array for one or more bit flips.

15. A method in accordance with claim 13 further comprising:

restoring said predetermined pattern after detecting a particle strike.

16. A method in accordance with claim 13 further comprising:

determining an angle of incidence of said particle strike from a pattern of bit flips in said plurality of layers caused by said particle strike.

17. A method in accordance with claim 16 wherein determining an angle of incidence comprises analyzing bit flips on each layer of memory cells.

18. A radiation detector comprising:

a microelectronic detection circuit configured to change state in response to radiation; and

a microprocessor connected to said detection circuit responsive to changes in state of said detection circuit configured to report detection.

19. A radiation detector in accordance with claim 18 wherein said microelectronic detection circuit is further configured to detect secondary interactions caused by radiation.

20. A radiation detector in accordance with claim 18 wherein said microelectronic detection circuit is coated with a material to enhance detection of radiation.

21. A radiation detector in accordance with claim 18 wherein said microelectronic detection circuit comprises stacked arrays of detector circuits.

22. A radiation detector in accordance with claim 21 wherein each of said stacked arrays of detector circuits is coated with a material to enhance detection of radiation.

23. A radiation detector in accordance with claim 21 wherein each of said stacked arrays of detector circuits is sensitized to a particular radiation indicator.

24. A radiation detector in accordance with claim 18 wherein said microelectronic detection circuit is selected from a group comprising SRAM, DRAM, EEPROM and diodes.